Please add new claim 11 as follows:

11. A digital broadcast demodulator according to claim 1, wherein said polarity of said polarity of the most significant bit (MSB) of the reception transport packet data is either positive or negative.

REMARKS

I. Introduction

In response to the pending rejection, Applicants have amended claims 1, 4, 7, 8 and 10 so as to address the rejection of the same under 35 U.S.C. § 112, second paragraph. New claim 11 has been added. In addition, Applicants have amended the Abstract such that it complies with the requirement of being only a single paragraph. Figs. 1 and 10 have been amended to address the objections thereto raised in paragraphs 1-3 of the Office Action, and Fig. 9 has also be amended so as to correctly illustrate the circuitry set forth in the specification. It is noted that Figs. 1 and 10 have been revised to include descriptions of each block set forth therein. However, as none of the circuits set forth in Fig. 9 included descriptions, none have been added. It is noted that each of the circuits illustrated in Fig. 9 is described in the specification (*see*, pages 13 and 14 of the specification). Once the amendments to the drawings have been approved, revised formal drawings will be submitted. No new matter has been added.

It is further noted that in response to the question set forth in paragraph 3 of the Office Action, the circuit recited by claim 6 corresponds to circuit 105 of Fig. 1, which is explained in detail in Fig. 9 and the corresponding portion of the specification.

For the reasons set forth below, Applicants respectfully submit that all pending claims are now in condition for allowance.

Applicants note with appreciation, the indication of allowable subject matter being recited by claims 2, 3, 5, 6 and 9.

II. The Rejection Of The Claims Under 35 U.S.C. § 112,

Claims 1, 4, 7, 8 and 10 were rejected under 35 U.S.C. § 112, second paragraph for being indefinite. In response, Applicants have amended each of the foregoing claims so as to address each of the alleged indefinite terms, which are identified in paragraph 5 of the Office Action. It is respectfully submitted that, as amended, each of the foregoing claims is definite and readily understandable by one of skill in the art, when read in light of the specification. Accordingly, it is respectfully submitted that the claims, as amended, fully comply with the requirements of 35 U.S.C. § 112, second paragraph. As such, Applicants respectfully submit that the pending rejection under 35 U.S.C. § 112, ¶ 2 has been overcome.

III. Rejection Of Claims 1, 4 And 7 Under 35 U.S.C. § 102

Claims 1, 4 and 7 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,508,748 to Krishnamurthy. Applicants respectfully submit that the claims are patentable over Krishnamurthy for at least the following reasons.

As recited by claim 1, the digital broadcast demodulator of the present invention comprises a circuit for establishing a synchronous signal in reception data ***based on the polarity of*** the most significant bit (MSB) of the reception transport packet data, where the polarity can be either positive or negative. The operation of the foregoing circuit is detailed, for example, on pages 8 and 9 of the specification.

In the pending rejection, the "slicer & error" generator circuit 36 of Krishnamurthy is cited as performing the foregoing function. However, it does not appear that the circuit 36 of Krishnamurthy, which is illustrated in detail in Fig. 5, utilizes or considers the polarity the most significant bit (MSB) of the reception transport packet data when establishing the synchronous signal. It is further noted that the portions of Krishnamurthy cited in the pending rejection also fail to mention or suggest utilization of the polarity of the MSB of the transport packet data to establish the synchronous signal.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is clear that Krishnamurthy

does not anticipate claim 1.

Claim 4 of the present invention recites the determination of a differential value of synchronous signals of reception packet data, which is then utilized to detect a clock phase error of the transmission data. The clock signal is regenerated by performing phase control on the basis of the clock phase error. More specifically, referring to pages 12-14 of the specification, in accordance with the embodiment encompassed by claim 4, a clock phase error associated with received data is determined by calculating the difference between the Nth and Nth+1 packet synchronous signals of the received data, and then this difference value is utilized (i.e., the clock phase error) to generate the clock signal.

In the pending rejection, the divider 52 of Krishnamurthy is cited as performing the foregoing limitation recited by claim 4. Applicants respectfully disagree. At a minimum, divider 52 of Krishnamurthy does not appear to generate any clock phase error signal based on a comparison of synchronous signals of the reception packet data. As such, the divider of Krishnamurthy cannot be properly relied upon as disclosing the present invention as recited by claim 4. Thus, it is respectfully submitted that claim 4 is not anticipated by Krishnamurthy.

Finally, it is noted that for at least the same reasons of claim 4, Krishnamurthy also fails to anticipate claim 7.

For all of the foregoing reasons, it is respectfully submitted that claims 1, 4 and 7 are not anticipated by Krishnamurthy.

IV. Rejection Of Claim 1 Under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,602,595 to Citta. Applicants respectfully submit that claim 1 is patentable over Citta for at least the following reasons.

As mentioned above, claim 1 recites a digital broadcast demodulator comprising a circuit for establishing a synchronous signal in reception data ***based on the polarity of*** the most significant bit (MSB) of the reception transport packet data, where the polarity can be either positive or negative. The operation of the foregoing circuit is detailed, for example, on pages 8 and 9 of the specification.

Turning to the pending rejection, the "sync and timing" circuit 42 of Citta is cited as performing the foregoing function. However, it does not appear that the circuit 42 of Citta utilizes or considers the polarity the most significant bit (MSB) of the reception transport packet data when establishing the synchronous signal. It is further noted that the portions of Citta cited in the pending rejection also fail to mention or suggest utilization of the polarity of the MSB of the transport packet data to establish the synchronous signal.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is also clear that Citta does not anticipate claim 1.

V. Rejection Of Claims 8 And 10 Under 35 U.S.C. § 103

Claims 8 and 10 were rejected under 35 U.S.C. § 103 as being obvious in view of USP No. 5,602,595 to Citta. Applicants respectfully submit that claims 8 and 10 are patentable over Citta for at least the following reasons.

As recited by pending claim 8, as detailed on pages 15 and 16 of the specification, when the synchronous signal is detected in the received packet data, the difference between the data value of the synchronous signal and a reference value is determined, and this difference value is then utilized to determine the automatic gain control so as to adjust the difference value to zero.

Turning to the pending rejection, it is asserted that although Citta does not disclose AGC control it would be obvious to modify the reference to include such control. Applicants respectfully disagree. First, Applicants are not merely attempting to claim AGC as novel. It is the combination of the generation of the difference signal (which is based on the difference between the synchronous signal and the reference

value) and the utilization of this difference signal to perform the AGC in a digital broadcast demodulator that the Applicants believe to be novel. Second, it does not appear that Citta even discloses the generation of the claimed difference signal.

Thus, as each and every limitation of the pending claim must be disclosed or suggested by the prior art in order to establish a *prima facie* case of obviousness (see, M.P.E.P. § 2143.03), and for at least the foregoing reasons, Citta fails to do so, it is respectfully submitted that claim 8 is patentable over Citta.

Moreover, it is well known that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. ***In re Deminski***, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).

Indeed, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. ***In re Warner***, 379 F.2d 1011, 154, USPQ 173 (CCPA 1967).

For all of the foregoing reasons, it is respectfully submitted that claim 8 is patentable over Citta. It is further submitted that claim 10 is patentable for at least the same reasons.

VI. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Attached hereto is a clean version of the title of the invention, specification and claims by the current amendment. The attached page is captioned "**Appendix.**"

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 2/5/03

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APPENDIX

IN THE ABSTRACT:

The second paragraph has been deleted of the originally filed Abstract, which begins of line 17 of page 23 of the specification.

IN THE CLAIMS:

Claims 1, 4, 7, 8 and 10 have been amended as follows:

1. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form, comprising:

a circuit for establishing a synchronous signal in reception data based on a polarity of the most significant bit (MSB) of the reception transport packet data.

4. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein a differential value of synchronous signals of reception packet data is determined so as to detect a clock phase error of transmission data, and a clock signal is regenerated by phase control on the basis of said clock phase error.

7. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB

modulation system in packet form,

wherein a clock signal is regenerated by detecting a clock phase error from a differential value of the data coinciding with a synchronous signal code pattern of reception data until the synchronous signal of reception packet data is detected and established.

8. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein a synchronous signal in the received packet data is detected, the difference between the detected data value of the synchronous signal and a predetermined reference value is determined, and automatic gain control is performed on the basis of this difference.

10. A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein automatic gain control is performed by detecting the amplitude difference from an envelope of analog detected base band signal until a synchronous signal of reception packet data is detected and established.

New claim 11 have been added as follows:

11. A digital broadcast demodulator according to claim 1, wherein said polarity of said polarity of the most significant bit (MSB) of the reception transport packet data is either positive or negative.